Identical Inventive Entities

13/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015015607 **Image available**
WPI Acc No: 2003-076124/200307
XRPX Acc No: N03-058977
Wafer prober **has a chuck top** conductive layer **formed over one principle face of a** ceramic **substrate**
Patent Assignee: IBIDEN CO LTD (IBIG); HIRAMATSU Y (HIRA-I); ITO A (ITOA-I); ITO Y (ITOY-I)
Inventor: **HIRAMATSU Y** ; **ITO A** ; **ITO Y** ; ITO A
Number of Countries: 022 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 2002101816	A1	20021219	WO 2001JP4775	A	20010606	200307 B
US 20040021475	A1	20040205	WO 2001JP4775	A	20010606	200411
			US 2003343747	A	20030827	
EP 1394847	A1	20040303	EP 2001936871	A	20010606	200417
			WO 2001JP4775	A	20010606	

Priority Applications (No Type Date): WO 2001JP4775 A 20010606
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 2002101816	A1	J	36	H01L-021/66	
Designated States (National): IL US					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR					
US 20040021475	A1			G01R-031/02	
EP 1394847	A1	E		H01L-021/66	Based on patent WO 2002101816
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR					

Wafer prober **has a chuck top** conductive layer **formed over one principle face of a** ceramic **substrate**
Inventor: **HIRAMATSU Y** ...

... **ITO A** ...

... **ITO Y**

Abstract (Basic):
... **Wafer prober** has a chuck top **conductive layer** formed over one principal face of a **ceramic** substrate, and a guard electrode is formed therein. The **wafer prober** is characterized in that a metal layer is formed on the side face of the **ceramic** substrate.
... **Wafer prober** is capable of protecting a chuck top **conductive layer** against noises and preventing an erroneous action, as caused by the noises, of a semiconductor
...Title Terms: **CERAMIC** ;

13/3,K/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014269007
WPI Acc No: 2002-089705/200212
XRAM Acc No: C02-027615
XRPX Acc No: N02-066131

Ceramic **substrate used as electrostatic chuck,** wafer prober **or hot plate has a specified ratio of average** conductive - layer **thickness to an average** ceramic -**substrate thickness**

Patent Assignee: IBIDEN CO LTD (IBIG); HIRAMATSU Y (HIRA-I); ITO Y (ITOY-I)

Inventor: **HIRAMATSU Y ; ITO Y**

Number of Countries: 022 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200182366	A1	20011101	WO 2001JP3299	A	20010418	200212 B
JP 2001302330	A	20011031	JP 2000121938	A	20000424	200212
US 20020158328	A1	20021031	WO 2001JP3299	A	20010418	200274
			US 2002926800	A	20020319	
EP 1286390	A1	20030226	EP 2001921864	A	20010418	200319
			WO 2001JP3299	A	20010418	
JP 2003289027	A	20031010	JP 2000121938	A	20000424	200367
			JP 2002342764	A	20000424	
US 20040007773	A1	20040115	WO 2001JP3299	A	20010418	200406
			US 2002926800	A	20020319	
			US 2003615950	A	20030710	
US 6753601	B2	20040622	WO 2001JP3299	A	20010418	200445
			US 2002926800	A	20020319	

Priority Applications (No Type Date): JP 2000121938 A 20000424; JP 2002342764 A 20000424

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200182366	A1	J	58	H01L-021/68	
Designated States (National): US					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR					
JP 2001302330	A		20	C04B-035/00	
US 20020158328	A1			H01L-023/53	
EP 1286390	A1	E		H01L-021/68	Based on patent WO 200182366
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR					
JP 2003289027	A		20	H01L-021/02	Div ex application JP 2000121938
US 20040007773	A1			B32B-003/00	Cont of application WO 2001JP3299 Cont of application US 2002926800
US 6753601	B2			H01L-023/06	Based on patent WO 200182366

Ceramic **substrate used as electrostatic chuck,** wafer prober **or hot plate has a specified ratio of average** conductive - layer **thickness to an average** ceramic -**substrate thickness**

Inventor: **HIRAMATSU Y** ...

... **ITO Y**

Abstract (Basic):

... **Ceramic** substrate has a **conductive layer** disposed on its surface or inside it. A ratio (t2/t1) of a average **conductive** - **layer** thickness (t2) to an average **ceramic** -substrate thickness (t1) is less than 0.1, and variations in thickness from an average **conductive** - **layer** thickness range from 70 to +150%.

... **Ceramic** substrate is free from cracking or warping on heating or cooling quickly, from location-dependent variations in chucking force when the **ceramic** substrate constitutes an electrostatic chuck, from location-dependent variations in wafer treatment surface temperature when the **ceramic** substrate constitutes a hot plate, and from variations in voltage applied to guard electrodes or ground

electrodes when the **ceramic substrate** constitutes a **wafer prober** to permit the removal of stray capacity or noise...

...The **ceramic** substrate is used as electrostatic chuck, **wafer prober** or hot plate
Title Terms: **CERAMIC** ;

13/3,K/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014025281 **Image available**
WPI Acc No: 2001-509495/200156
XRPX Acc No: N01-378754
Wafer probe has electric power unit that impresses voltage so that specific potential will be generated in upper conductor layer and ground electrodes
Patent Assignee: IBIDEN CO LTD (IBIG)
Inventor: **HIRAMATSU Y** ; **ITO A** ; **ITO Y**
Number of Countries: 021 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001196426	A	20010719	JP 2000318064	A	20001018	200156	B
WO 200235603	A1	20020502	WO 2001JP3770	A	20010501	200236	

Priority Applications (No Type Date): JP 99302520 A 19991025
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001196426	A		15	H01L-021/66	
WO 200235603	A1	J		H01L-021/66	

Designated States (National): US
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

Wafer probe has electric power unit that impresses voltage so that specific potential will be generated in upper conductor layer and ground electrodes
Inventor: **HIRAMATSU Y** ...

... **ITO A** ...

... **ITO Y**

Abstract (Basic):
... An upper **conductor layer** (2) is formed on the surface of a **ceramic** substrate (3) in which ground electrodes (5) are arranged. An electric power unit impresses a voltage to generate a specific potential in the upper **conductor layer** and ground electrodes.
... An INDEPENDENT CLAIM is also included for a **ceramic** substrate used for a **wafer probe** .
...

...The figure is the sectional view of the **wafer probe** .
...
...Upper **conductor layer** (2...

... **Ceramic** substrate (3

13/3,K/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013663159 **Image available**
WPI Acc No: 2001-147371/200115
XRPX Acc No: N01-107870
Wafer prober **includes** conductor layer **formed on surface of** ceramic **substrate**
Patent Assignee: IBIDEN CO LTD (IBIG)
Inventor: **FURUKAWA M** ; **HIRAMATSU Y** ; **ITO A** ; **ITO Y**
Number of Countries: 026 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200106559	A1	20010125	WO 99JP5693	A	19991015	200115	B
EP 1091400	A1	20010411	EP 99949311	A	19991015	200121	
			WO 99JP5693	A	19991015		
JP 2001033484	A	20010209	JP 99201789	A	19990715	200124	
CN 1329753	A	20020102	CN 99814050	A	19991015	200227	
TW 449845	A	20010811	TW 99118768	A	19991029	200237	
KR 2002011850	A	20020209	KR 2000711162	A	20001007	200257	
JP 2003133374	A	20030509	JP 99201789	A	19990715	200339	
			JP 2002313295	A	19990715		

Priority Applications (No Type Date): JP 99201789 A 19990715; JP 2002313295 A 19990715
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200106559	A1	J	39	H01L-021/66	
Designated States (National): CN IL KR SG US					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
EP 1091400	A1	E			Based on patent WO 200106559
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
JP 2001033484	A		14	G01R-001/073	
CN 1329753	A			H01L-021/66	
TW 449845	A			H01L-021/66	
KR 2002011850	A			H01L-021/66	
JP 2003133374	A		13	H01L-021/66	Div ex application JP 99201789

Wafer prober **includes** conductor layer **formed on surface of** ceramic **substrate**
Inventor: **FURUKAWA M** ...

... **HIRAMATSU Y** ...
... **ITO A** ...

... **ITO Y**

Abstract (Basic):
... A lightweight **wafer prober** of good temperature characteristic, which is unlikely to warp when its probe card is pressed, thereby effectively preventing damage to silicon wafers and measurement errors. The **wafer prober** includes a **conductor layer** formed on the surface of a **ceramic** substrate.
... **Wafer prober** includes **conductor layer** formed on surface of **ceramic** substrate
...Title Terms: **CERAMIC** ;

13/3,K/5 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

08040529 **Image available**
WAFER PROBER DEVICE

PUB. NO.: 2004-153288 [JP 2004153288 A]
PUBLISHED: May 27, 2004 (20040527)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2003-407989 [JP 2003407989]
Division of 2000-251087 [JP 2000251087]
FILED: December 05, 2003 (20031205)
PRIORITY: 11-236143 [JP 99236143], JP (Japan), August 23, 1999 (19990823)

WAFER PROBER DEVICE

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide **wafer prober** device that has no warp, even if a probe card is pressed, can effectively protect...

... is light-weight and superior in a temperature rise and fall characteristic.

SOLUTION: This is **wafer prober** device composed of a **ceramic** substrate on whose surface a **conductor layer** is formed and its support container, and a support column is built up in the container. **Wafer prober** device can be obtained, even when a probe card is pressed, there occurs no warp...

13/3,K/6 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

07999235 **Image available**
WAFER PROBER AND **CERAMIC SUBSTRATE** USED FOR THE SAME

PUB. NO.: 2004-111994 [JP 2004111994 A]
PUBLISHED: April 08, 2004 (20040408)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2003-407990 [JP 2003407990]
Division of 2000-251088 [JP 2000251088]
FILED: December 05, 2003 (20031205)
PRIORITY: 11-236144 [JP 99236144], JP (Japan), August 23, 1999 (19990823)

WAFER PROBER AND **CERAMIC SUBSTRATE** USED FOR THE SAME

INVENTOR(s): **ITO ATSUSHI**

HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **ceramic** substrate which is hardly warped when a probe card is pressed against it, capable of...

... equipped with electrodes that are separately controlled, and excellent in controllability.

SOLUTION: A chuck top **conductor layer** is formed on the surface of the **ceramic** substrate, a guard electrode and/or a ground electrode is formed inside the **ceramic** substrate, and through-holes are formed in the **ceramic** substrate, which are electrically connected to either or both of the guard electrode and the...

13/3,K/7 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

07991393 **Image available**
WAFER PROBER APPARATUS

PUB. NO.: 2004-104152 [JP 2004104152 A]
PUBLISHED: April 02, 2004 (20040402)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2003-407992 [JP 2003407992]
Division of 2000-251111 [JP 2000251111]
FILED: December 05, 2003 (20031205)
PRIORITY: 11-236146 [JP 99236146], JP (Japan), August 23, 1999 (19990823)

WAFER PROBER APPARATUS

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **wafer prober** apparatus which can efficiently and rapidly heat/cool a **wafer prober**, can control its temperature and can effectively prevent a silicon wafer from being damaged or...

...mistake without bringing about a warp even when a probe card is pressed.

SOLUTION: The **wafer prober** apparatus includes a **conductor layer** formed on a surface, a **ceramic** substrate having a heating means, and a support container. A liquid jet port is formed...

13/3,K/8 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO

07991392 **Image available**
WAFER PROBER

PUB. NO.: 2004-104151 [JP 2004104151 A]
PUBLISHED: April 02, 2004 (20040402)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2003-407991 [JP 2003407991]
Division of 2000-251110 [JP 2000251110]
FILED: December 05, 2003 (20031205)
PRIORITY: 11-236145 [JP 99236145], JP (Japan), August 23, 1999 (19990823)

WAFER PROBER

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **wafer prober** which has excellent controllability without warp even when a probe card is pressed without release...

... damaged or measured by mistake, and which has excellent temperature rise/fall characteristics.

SOLUTION: The **wafer prober** in which a chuck top **conductor layer** is formed on a surface of a **ceramic** substrate and a guard electrode and/or a ground electrode is formed in the **substrate** . In the **prober** , one or both of the guard electrode and the ground electrode is electrically connected. The...

13/3,K/9 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

07991391 **Image available**
WAFER PROBER AND **CERAMIC SUBSTRATE** USED THEREFOR

PUB. NO.: 2004-104150 [JP 2004104150 A]
PUBLISHED: April 02, 2004 (20040402)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2003-407988 [JP 2003407988]
Division of 2000-248580 [JP 2000248580]
FILED: December 05, 2003 (20031205)
PRIORITY: 11-233117 [JP 99233117], JP (Japan), August 19, 1999 (19990819)

WAFER PROBER AND **CERAMIC SUBSTRATE** USED THEREFOR

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **ceramic** substrate having a chuck top **conductor layer** which is thin, excellent adhesive properties with the substrate and which reduces the resistance.

SOLUTION: The **ceramic** substrate used for a **wafer prober** includes a **conductor layer** made of a plurality of metal layers.

13/3,K/10 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO

07975358 **Image available**
WAFER PROBER AND **CERAMIC SUBSTRATE** FOR USE IN **WAFER PROBER**

PUB. NO.: 2004-088117 [JP 2004088117 A]
PUBLISHED: March 18, 2004 (20040318)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2003-346154 [JP 2003346154]
Division of 2000-254183 [JP 2000254183]
FILED: October 03, 2003 (20031003)
PRIORITY: 11-238958 [JP 99238958], JP (Japan), August 25, 1999 (19990825)

WAFER PROBER AND **CERAMIC SUBSTRATE** FOR USE IN **WAFER PROBER**

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **ceramic** substrate for use in a **wafer prober** wherein warp is not produced even at high temperature; even if a silicon wafer is placed on a chuck top **conductor layer** for continuity test, the silicon wafer is not damaged; and the **ceramic** wafer can be increased in size and reduced in thickness.

SOLUTION: The **ceramic** substrate is for use in a **wafer prober** . The chuck top **conductor layer** is formed over one principal surface of the **ceramic** substrate, and a **conductor layer** is formed over the other principal surface.

13/3,K/11 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO

07755627 **Image available**
WAFER PROBER , AND **CERAMIC** BOARD USED FOR **WAFER PROBER**

PUB. NO.: 2003-249533 [JP 2003249533 A]
PUBLISHED: September 05, 2003 (20030905)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2002-356539 [JP 2002356539]

Division of 2000-318066 [JP 2000318066]
FILED: October 18, 2000 (20001018)
PRIORITY: 11-306566 [JP 99306566], JP (Japan), October 28, 1999 (19991028)

WAFER PROBER, AND **CERAMIC** BOARD USED FOR **WAFER PROBER**

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **wafer prober** where the heat conduction from the side of a **ceramic** board to a support container is suppressed and the temperature of a chuck top **conductor layer**, on which to place a silicon wafer, is equalized, when the temperature of the **ceramic** board is raised and also a side conductor can be formed properly.

SOLUTION: In the **wafer prober**, where the chuck top **conductor layer** is formed on the surface of the **ceramic** board, the face roughness, based on JIS R 0601 of the flank adjacent to the face where the above chuck top **conductor layer** is made, is Rmax=0.2-200 μm.

13/3,K/12 (Item 12 from file: 347)

07749556 **Image available**
WAFER PROBER AND CERAMIC SUBSTRATE FOR USE THEREIN

PUB. NO.: 2003-243461 [JP 2003243461 A]
PUBLISHED: August 29, 2003 (20030829)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2002-356538 [JP 2002356538]
Division of 2000-318065 [JP 2000318065]
FILED: October 18, 2000 (20001018)
PRIORITY: 11-303806 [JP 99303806], JP (Japan), October 26, 1999 (19991026)

WAFER PROBER AND CERAMIC SUBSTRATE FOR USE THEREIN

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **wafer prober** in which a **ceramic** substrate is protected against damage due to the difference of thermal expansion between a guard electrode and/or a ground electrode and surrounding **ceramic**, variation in the conductivity of the electrode due to the reaction of the surrounding **ceramic** and the guard electrode or the like, is suppressed even when a temperature rises up...

...through hole is prevented from being stripped from a bonding interface.

SOLUTION: A chuck top **conductor layer** is formed on the surface of a

ceramic substrate, and a guard electrode and/or a ground electrode are/is formed in the **ceramic** substrate and connected with a through hole. The guard electrode and/or the ground electrode are/is composed of conductive **ceramic** at least partially and the through hole is composed of a high melting point metal...

13/3,K/13 (Item 13 from file: 347)
DIALOG(R)File 347:JAPIO

07740484 **Image available**
WAFER PROBER AND **CERAMIC SUBSTRATE** FOR USE IN **WAFER PROBER**

PUB. NO.: 2003-234386 [JP 2003234386 A]
PUBLISHED: August 22, 2003 (20030822)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2003-027277 [JP 200327277]
Division of 2000-322987 [JP 2000322987]
FILED: October 23, 2000 (20001023)
PRIORITY: 11-303808 [JP 99303808], JP (Japan), October 26, 1999 (19991026)

WAFER PROBER AND **CERAMIC SUBSTRATE** FOR USE IN **WAFER PROBER**

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **wafer prober** which has high thermal conductivity at high temperatures a superior temperature rise and fall characteristics...

... heat for heating a silicon wafer, and ensure thermal conductivity at high temperatures.

SOLUTION: A **ceramic** substrate for use in **wafer probers** has a chuck top **conductor layer** formed on its surface, and the **ceramic** substrate contains carbon.

13/3,K/14 (Item 14 from file: 347)
DIALOG(R)File 347:JAPIO

07710059 **Image available**
WAFER PROBER AND **CERAMIC SUBSTRATE** THEREFOR

PUB. NO.: 2003-203955 [JP 2003203955 A]
PUBLISHED: July 18, 2003 (20030718)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2002-356537 [JP 2002356537]

Division of 2000-313460 [JP 2000313460]
FILED: October 13, 2000 (20001013)
PRIORITY: 11-304547 [JP 99304547], JP (Japan), October 26, 1999 (19991026)

WAFER PROBER AND **CERAMIC SUBSTRATE** THEREFOR

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **ceramic** substrate which is fully blackened, capable of concealing a guard electrode and a gland electrode, as well as ensuring thermal conductivity and volume resistivity sufficient to function as a **wafer prober** .

SOLUTION: The **ceramic substrate** for the **wafer prober** with a chuck top **conductor layer** formed on the surface thereof is provided, wherein an X-ray diffraction chart of the **ceramic** substrate, in addition to a peak of the **ceramic** constituting a main crystal phase thereof, a peak of carbon is detected to an angle...

13/3,K/15 (Item 15 from file: 347)
DIALOG(R)File 347:JAPIO

07581664 **Image available**
WAFER PROBER AND **CERAMIC** BOARD USED IN **WAFER PROBER**

PUB. NO.: 2003-075507 [JP 2003075507 A]
PUBLISHED: March 12, 2003 (20030312)
INVENTOR(s): **ITO YASUTAKA**
HIRAMATSU YASUJI
FURUKAWA KAZUMASA
ITO ATSUSHI
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2002-227783 [JP 2002227783]
Division of 2000-240815 [JP 2000240815]
FILED: August 09, 2000 (20000809)
PRIORITY: 11-227778 [JP 99227778], JP (Japan), August 11, 1999 (19990811)

WAFER PROBER AND **CERAMIC** BOARD USED IN **WAFER PROBER**

INVENTOR(s): **ITO YASUTAKA**
HIRAMATSU YASUJI
FURUKAWA KAZUMASA
ITO ATSUSHI

ABSTRACT

PROBLEM TO BE SOLVED: To provide a lightweight **wafer prober** having superior temperature rise and drop characteristic, causing no warp even in the case where...

... pressed, and effectively preventing breakage of silicon wafer and a measuring error.

SOLUTION: In this **wafer prober** , a **conductor layer** is formed on the surface of the **ceramic** board, and it is characterized in that the

conductor layer is thinner than the **ceramic** board.

13/3,K/16 (Item 16 from file: 347)
DIALOG(R)File 347:JAPIO

07002667 **Image available**
WAFER PROBER

PUB. NO.: 2001-230284 [JP 2001230284 A]
PUBLISHED: August 24, 2001 (20010824)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
FURUKAWA MASAKAZU
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2000-034980 [JP 200034980]
FILED: February 14, 2000 (20000214)

WAFER PROBER

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
FURUKAWA MASAKAZU

ABSTRACT
PROBLEM TO BE SOLVED: To provide a **wafer prober** with a chuck top **conductive layer** hardly flaked from a **ceramic** board.

SOLUTION: In the **wafer prober** , the chuck top **conductive layer** is formed on the surface of the **ceramic** board. The surface roughness of at least a face where the chuck top layer is...

13/3,K/17 (Item 17 from file: 347)
DIALOG(R)File 347:JAPIO

06995669 **Image available**
WAFER PROBER AND STAGE FOR INSPECTION USED FOR THE SAME

PUB. NO.: 2001-223249 [JP 2001223249 A]
PUBLISHED: August 17, 2001 (20010817)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2000-358392 [JP 2000358392]
FILED: November 24, 2000 (20001124)
PRIORITY: 11-335639 [JP 99335639], JP (Japan), November 26, 1999 (19991126)

WAFER PROBER AND STAGE FOR INSPECTION USED FOR THE SAME

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI

ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **wafer prober** with a stage for inspection having excellent heating efficiency by using a **ceramic** material in which lightness is set N4 or less by the standard of JIS 28721.

SOLUTION: The stage 12 for inspection is composed of the **ceramic** material such as aluminum nitride, in which lightness is set N4 or less by the...

...is formed on the surface of the stage 12 for inspection as a chuck-top **conductor layer** 14.

13/3,K/18 (Item 18 from file: 347)

06995668 **Image available**

WAFER PROBER AND STAGE FOR INSPECTION USED THE SAME

PUB. NO.: 2001-223248 [JP 2001223248 A]
PUBLISHED: August 17, 2001 (20010817)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2000-358391 [JP 2000358391]
FILED: November 24, 2000 (20001124)
PRIORITY: 11-333548 [JP 99333548], JP (Japan), November 25, 1999 (19991125)

WAFER PROBER AND STAGE FOR INSPECTION USED THE SAME

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **wafer prober** in which the reliability of electrical connection with through-holes formed among an external terminal...

...to the surface or inside of a stage for inspection is improved.

SOLUTION: Chuck-top **conductor layers** 36 are formed onto the surface of a **ceramic** stage 12 on which a semiconductor wafer is placed, and electrodes 14, 16 are formed into the **ceramic** stage 12 while through-holes 20, 22 electrically connecting the electrodes 14, 16 and the ...

13/3,K/19 (Item 19 from file: 347)

06983112 **Image available**

WAFER PROBER AND **CERAMIC SUBSTRATE** FOR USE IN **WAFER PROBERS**

PUB. NO.: 2001-210686 [JP 2001210686 A]
PUBLISHED: August 03, 2001 (20010803)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2000-322987 [JP 2000322987]
FILED: October 23, 2000 (20001023)
PRIORITY: 11-303808 [JP 99303808], JP (Japan), October 26, 1999 (19991026)

WAFER PROBER AND **CERAMIC SUBSTRATE** FOR USE IN **WAFER PROBERS**

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **wafer prober** which has a high thermal conductivity at high temperatures and superior temperature rise and fall...

... heats for heating silicon wafers, and ensure a thermal conductivity at high temperatures.

SOLUTION: The **ceramic** substrate for use in **wafer probers** has a chuck top **conductor layer** formed on its surface and the **ceramic** substrate characteristically contains carbon.

13/3,K/20 (Item 20 from file: 347)
DIALOG(R)File 347:JAPIO

06975674 **Image available**
WAFER PROBER AND **CERAMIC SUBSTRATE** USED THEREFOR

PUB. NO.: 2001-203245 [JP 2001203245 A]
PUBLISHED: July 27, 2001 (20010727)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2000-306853 [JP 2000306853]
FILED: August 30, 2000 (20000830)
PRIORITY: 11-243112 [JP 99243112], JP (Japan), August 30, 1999 (19990830)
11-316333 [JP 99316333], JP (Japan), November 08, 1999 (19991108)

WAFER PROBER AND **CERAMIC SUBSTRATE** USED THEREFOR

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a light **wafer prober** with improved

durability.

SOLUTION: In the **wafer prober** used for inspecting the continuity of an integrated circuit formed on a semiconductor wafer, a **conductor layer** that is made of a metal material containing phosphor or boron is formed on the surface of an inspection stage that is made of a **ceramic** material for placing the semiconductor wafer to be inspected.

13/3,K/21 (Item 21 from file: 347)
DIALOG(R)File 347:JAPIO

06968858 **Image available**
WAFER PROBER AND **CERAMIC** BOARD USED THEREFOR

PUB. NO.: 2001-196428 [JP 2001196428 A]
PUBLISHED: July 19, 2001 (20010719)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2000-318066 [JP 2000318066]
FILED: October 18, 2000 (20001018)
PRIORITY: 11-306566 [JP 99306566], JP (Japan), October 28, 1999 (19991028)

WAFER PROBER AND **CERAMIC** BOARD USED THEREFOR

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **wafer prober**, where heat is restrained from being transferred from the side of a **ceramic** board to a support case even in a case in which a **ceramic** board is raised in temperature, a chuck top **conductor layer** on which a silicon wafer is placed is kept uniform in temperature, and a side conductor can be formed.

SOLUTION: A chuck top **conductor layer** is formed on the surface of a **ceramic** board for the formation of a **wafer prober**, where the surface roughness of the side of the **ceramic** board adjoining to its surface on which the **conductor layer** is formed is set at Rmax of 0.2 to 200 μm based on...

13/3,K/22 (Item 22 from file: 347)
DIALOG(R)File 347:JAPIO

06968857 **Image available**
WAFER PROBER AND **CERAMIC** BOARD USED FOR THE SAME

PUB. NO.: 2001-196427 [JP 2001196427 A]
PUBLISHED: July 19, 2001 (20010719)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI

ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2000-318065 [JP 2000318065]
FILED: October 18, 2000 (20001018)
PRIORITY: 11-303806 [JP 99303806], JP (Japan), October 26, 1999 (19991026)

WAFER PROBER AND **CERAMIC** BOARD USED FOR THE SAME

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT
PROBLEM TO BE SOLVED: To provide a **wafer prober** , wherein a **ceramic** board is hardly damaged due to a thermal expansion difference between a surrounding **ceramic** and a guard electrode and/or a ground electrode, the electrodes are hardly changed in conductivity due to the fact that a surrounding **ceramic** reacts on the electrodes even if temperature rises up to 500°C or above...

...a through-hole is hardly separated off at a joint interface.

SOLUTION: A chuck top **conductor layer** is formed on the surface of a **ceramic** board, a guard electrode and/or a ground electrode is formed inside the **ceramic** board, and a through-hole is connected to the guard electrode and/or the ground electrode for the formation of a **wafer prober** , the guard electrode and/or the ground electrode is, at least, partially formed of conductive **ceramics** , and the through-hole is formed of high-melting metal.

13/3,K/23 (Item 23 from file: 347)
DIALOG(R)File 347:JAPIO

06968855 **Image available**
WAFER PROBER AND **CERAMIC** BOARD USED FOR THE SAME

PUB. NO.: 2001-196425 [JP 2001196425 A]
PUBLISHED: July 19, 2001 (20010719)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2000-313461 [JP 2000313461]
FILED: October 13, 2000 (20001013)
PRIORITY: 11-302957 [JP 99302957], JP (Japan), October 25, 1999 (19991025)

WAFER PROBER AND **CERAMIC** BOARD USED FOR THE SAME

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT
PROBLEM TO BE SOLVED: To provide a **wafer prober** in which a **ceramic**

board is hardly separated from a guard electrode and/or a ground electrode due to the difference in thermal expansion between a surrounding **ceramic** and the guard electrode and/or the ground electrode.

SOLUTION: A chuck top **conductor layer** is formed on the surface of a **ceramic** board, a guard electrode and/or a ground electrode is provided on the **ceramic** board for the formation of a **wafer prober** , and at least the guard electrode and/or the ground electrode is, at least, partially...

13/3,K/24 (Item 24 from file: 347)
DIALOG(R)File 347:JAPIO

06968854 **Image available**
WAFER PROBER AND **CERAMIC** BOARD USED FOR THE SAME

PUB. NO.: 2001-196424 [JP 2001196424 A]
PUBLISHED: July 19, 2001 (20010719)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2000-313460 [JP 2000313460]
FILED: October 13, 2000 (20001013)
PRIORITY: 11-304547 [JP 99304547], JP (Japan), October 26, 1999 (19991026)

WAFER PROBER AND **CERAMIC** BOARD USED FOR THE SAME

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT
PROBLEM TO BE SOLVED: To provide a **ceramic** board which is turned black enough to cover a guard electrode and a ground electrode and high enough in thermal conductivity and volume resistivity to function as a **wafer prober** .

SOLUTION: A **ceramic** board is provided with a chuck top **conductor layer** on its surface. In the X-ray diffraction chart of the **ceramic** board, other than a peak of **ceramic** which forms a main crystal phase, a peak of carbon is detected at an X...

13/3,K/25 (Item 25 from file: 347)
DIALOG(R)File 347:JAPIO

06961807 **Image available**
CERAMIC SUBSTRATE FOR MANUFACTURING AND INSPECTION APPARATUS FOR SEMICONDUCTOR

PUB. NO.: 2001-189373 [JP 2001189373 A]
PUBLISHED: July 10, 2001 (20010710)
INVENTOR(s): **HIRAMATSU YASUJI**
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 11-372166 [JP 99372166]

FILED: December 28, 1999 (19991228)

CERAMIC SUBSTRATE FOR MANUFACTURING AND INSPECTION APPARATUS FOR SEMICONDUCTOR

INVENTOR(s): **HIRAMATSU YASUJI**
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **ceramic** substrate for devices for manufacturing and inspecting of semiconductor that have a high volume resistivity...

... accuracy by a thermoviewer, and is suitable as a hot plate, an electrostatic chuck, a **wafer prober** , a susceptor, and the like.

SOLUTION: In the **ceramic** substrate for the apparatus for manufacturing and inspecting of semiconductors, a **conductor layer** is arranged on a **ceramic** substrate containing carbon, where peaks appear near 1,580 cm-1 and 1,355 cm...

13/3,K/26 (Item 26 from file: 347)
DIALOG(R)File 347:JAPIO

06949386 **Image available**
WAFER PROBER

PUB. NO.: 2001-176938 [JP 2001176938 A]
PUBLISHED: June 29, 2001 (20010629)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 11-360614 [JP 99360614]
FILED: December 20, 1999 (19991220)

WAFER PROBER

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **wafer prober** which can protect a chuck top **conductor layer** from noises, and prevents a malfunction in an integrated circuit, etc., caused by these noises, and accurately determine whether or not the integrated circuit, etc., operates normally.

SOLUTION: In a **wafer prober** in which a chuck top **conductor layer** is formed on one major face of a **ceramic** substrate, and also a guard electrode is formed in the interior, a metal layer is formed on the side face of the **ceramic** substrate.

13/3,K/27 (Item 27 from file: 347)
DIALOG(R)File 347:JAPIO

06940606 **Image available**
WAFER PROBER

PUB. NO.: 2001-168155 [JP 2001168155 A]
PUBLISHED: June 22, 2001 (20010622)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 11-348139 [JP 99348139]
FILED: December 07, 1999 (19991207)

WAFER PROBER

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **wafer prober** superior in temperature rise and high temperature characteristics, which allows a **ceramic** substrate thin and hardly warping, even heated.

SOLUTION: In the **wafer prober** having a chuck top **conductor layer** formed on the surface of the **ceramic** substrate, the **ceramic** substrate has a Young's modulus of 280-350 GPa in a temperature range of...

13/3,K/28 (Item 28 from file: 347)
DIALOG(R)File 347:JAPIO

06920866 **Image available**
WAFER PROBER

PUB. NO.: 2001-148405 [JP 2001148405 A]
PUBLISHED: May 29, 2001 (20010529)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 11-328981 [JP 99328981]
FILED: November 19, 1999 (19991119)

WAFER PROBER

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **wafer prober** in which a dielectric breakdown is not caused in a predetermined temperature region (25°...
...enables temperature control with superior responsiveness.

SOLUTION: An inspection stage 12 is made of a **ceramic** material of which main component is aluminum nitride and which has a volume resistivity of...

...m in the temperature region of 25°C-500°C. A chuck-top **conductor layer** 14 is composed of nickel and the like formed on the surface of the inspection...

13/3,K/29 (Item 29 from file: 347)
DIALOG(R)File 347:JAPIO
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06916613 **Image available**
WAFER PROBER

PUB. NO.: 2001-144150 [JP 2001144150 A]
PUBLISHED: May 25, 2001 (20010525)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 11-324862 [JP 99324862]
FILED: November 16, 1999 (19991116)

WAFER PROBER

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **wafer prober** which is superior in durable characteristics, uniforms the temperature of a semiconductor wafer and a **ceramic** stage, can speedily change the resistance value of a heating wire, when current and voltage...

... value does not fluctuate, even if conduction testing is executed repeatedly.

SOLUTION: A chuck top **conductor layer** 36, constituted of nickel comprising phosphorus and/or boron, is formed on the surface of a **ceramic** stage 12 on which a semiconductor wafer is placed and which is formed of aluminum nitride. A tungsten wire is embedded in the **ceramic** stage 12 as a heating wire 18.

13/3,K/30 (Item 30 from file: 347)
DIALOG(R)File 347:JAPIO
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06908161 **Image available**
WAFER PROBER AND **CERAMIC SUBSTRATE** TO BE USED FOR **WAFER PROBER**

PUB. NO.: 2001-135686 [JP 2001135686 A]
PUBLISHED: May 18, 2001 (20010518)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2000-254183 [JP 2000254183]
FILED: August 24, 2000 (20000824)

PRIORITY: 11-238958 [JP 99238958], JP (Japan), August 25, 1999 (19990825)

WAFER PROBER AND **CERAMIC SUBSTRATE** TO BE USED FOR **WAFER PROBER**

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a large-scaled thin **ceramic** substrate to be used for a **wafer prober** for preventing generation of bending even when it is exposed in a high temperature, and...

... silicon wafer even at the time of placing the silicon wafer on a chuck top **conductive layer** , and operating a continuity test.

SOLUTION: A chuck top **conductive** layer is formed on one main face of a **ceramic** substrate, and a **conductive layer** is formed on the other main face so that a **ceramic** substrate to be used for a **wafer prober** can be constituted.

13/3,K/31 (Item 31 from file: 347)

06908160 **Image available**
WAFER PROBER

PUB. NO.: 2001-135685 [JP 2001135685 A]
PUBLISHED: May 18, 2001 (20010518)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2000-254182 [JP 2000254182]
FILED: August 24, 2000 (20000824)
PRIORITY: 11-238959 [JP 99238959], JP (Japan), August 25, 1999 (19990825)

WAFER PROBER

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **wafer prober** for uniformly sucking the whole part of a silicon wafer without damaging the silicon wafer...

...the position of the tester pin of a probe card.

SOLUTION: A porous chuck top **conductive layer** 2 is formed on a pedestal constituted of a **ceramic** substrate 3 at which through-holes 8 for suction are formed so that a **wafer prober** can be constituted.

13/3,K/32 (Item 32 from file: 347)
DIALOG(R)File 347:JAPIO

06908159 **Image available**
WAFER PROBER DEVICE

PUB. NO.: 2001-135684 [JP 2001135684 A]
PUBLISHED: May 18, 2001 (20010518)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2000-251111 [JP 2000251111]
FILED: August 22, 2000 (20000822)
PRIORITY: 11-236146 [JP 99236146], JP (Japan), August 23, 1999 (19990823)

WAFER PROBER DEVICE

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a light **wafer prober** for efficiently and quickly heating and cooling a **wafer prober** , and for controlling the temperature, and for preventing generation of bending even at the time...

...a silicon wafer or measurement error.

SOLUTION: This wave prober device is constituted of a **ceramic** substrate on whose surface a **conductive layer** is formed, and at which a heating means is arranged and a support container, and...

13/3,K/33 (Item 33 from file: 347)
DIALOG(R)File 347:JAPIO

06908158 **Image available**
WAFER PROBER

PUB. NO.: 2001-135683 [JP 2001135683 A]
PUBLISHED: May 18, 2001 (20010518)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2000-251110 [JP 2000251110]
FILED: August 22, 2000 (20000822)
PRIORITY: 11-236145 [JP 99236145], JP (Japan), August 23, 1999 (19990823)

WAFER PROBER

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI

ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **wafer prober** with excellent controllability and temperature ascending and descending characteristics for preventing generation of peeling on...

...for preventing the damage to a silicon wafer or measurement error.

SOLUTION: A chuck top **conductive layer** is formed on the surface of a **ceramic** substrate, and a guard electrode and/or a ground electrode are formed inside the **ceramic substrate** so that **wafer prober** can be constituted. This **wafer prober** is provided with a through-hole electrically connected with one or both of the guard...

13/3,K/34 (Item 34 from file: 347)

06908157 **Image available**

WAFER PROBER AND **CERAMIC SUBSTRATE** TO BE USED THEREFOR

PUB. NO.: 2001-135682 [JP 2001135682 A]
PUBLISHED: May 18, 2001 (20010518)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2000-251088 [JP 2000251088]
FILED: August 22, 2000 (20000822)
PRIORITY: 11-236144 [JP 99236144], JP (Japan), August 23, 1999 (19990823)

WAFER PROBER AND **CERAMIC SUBSTRATE** TO BE USED THEREFOR

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **ceramic** substrate to be used for a **wafer prober** for preventing generation of bending even at the time of pressing a probe card, for...

... descending characteristics, and for improving controllability by individually controlling the electrode.

SOLUTION: A chuck top **conductive layer** is formed on the surface of a **ceramic** substrate, a guard electrode and/or a ground electrode is formed inside the **ceramic** substrate, and a through-hole is formed so as to be electrically connected with one...

... electrode, and so as to be electrically connected with an outside terminal so that a **ceramic** substrate to be used for a **wafer prober** can be constituted.

13/3,K/35 (Item 35 from file: 347)
DIALOG(R)File 347:JAPIO

06908156 **Image available**
WAFER PROBER DEVICE

PUB. NO.: 2001-135681 [JP 2001135681 A]
PUBLISHED: May 18, 2001 (20010518)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2000-251087 [JP 2000251087]
FILED: August 22, 2000 (20000822)
PRIORITY: 11-236143 [JP 99236143], JP (Japan), August 23, 1999 (19990823)

WAFER PROBER DEVICE

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT
PROBLEM TO BE SOLVED: To provide a **wafer prober** device with light weight and excellent temperature ascending and descending characteristics for preventing generation of...

...and for preventing the damage to a silicon wafer or measurement error.

SOLUTION: In this **wafer prober** device constituted of a **ceramic** substrate on whose surface a **conductive layer** is formed and a support container, supporting columns are formed in the support container.

13/3,K/36 (Item 36 from file: 347)
DIALOG(R)File 347:JAPIO

06908155 **Image available**
WAFER PROBER AND **CERAMIC SUBSTRATE** TO BE USED THEREFOR AND **WAFER PROBER** DEVICE

PUB. NO.: 2001-135680 [JP 2001135680 A]
PUBLISHED: May 18, 2001 (20010518)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2000-248582 [JP 2000248582]
FILED: August 18, 2000 (20000818)
PRIORITY: 11-230991 [JP 99230991], JP (Japan), August 18, 1999 (19990818)

WAFER PROBER AND **CERAMIC SUBSTRATE** TO BE USED THEREFOR AND **WAFER PROBER** DEVICE

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **ceramic** substrate to be used for a **wafer prober** with excellent temperature ascending and descending characteristics for preventing generation of bending without shifting a...

... tester pin, and for preventing the damage to the wafer or measurement error.

SOLUTION: A **conductive layer** 2 is formed on the surface of a **ceramic** substrate 3, and plural concentric circular grooves 7 are formed on the **ceramic** substrate 3, and through-holes 8 are formed at one pert of the grooves 7, and concentric circular heating elements 41 are arranged on the bottom face of the **ceramic** substrate 3 so that a **ceramic** substrate 3 to be used for a **wafer prober** 101 can be constituted.

13/3,K/37 (Item 37 from file: 347)

06899614 **Image available**
WAFER PROBER AND **CERAMIC SUBSTRATE** USED FOR THE SAME

PUB. NO.: 2001-127124 [JP 2001127124 A]
PUBLISHED: May 11, 2001 (20010511)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2000-248581 [JP 2000248581]
FILED: August 18, 2000 (20000818)
PRIORITY: 11-230990 [JP 99230990], JP (Japan), August 18, 1999 (19990818)

WAFER PROBER AND **CERAMIC SUBSTRATE** USED FOR THE SAME

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **ceramic** substrate used for a **wafer prober** which is light, has excellent characteristics in a temperature rise and drop, is not warped...

...or stray capacitance due to temperature control means or the like.

SOLUTION: A chuck top **conductor layer** is formed on the surface of this **ceramic** substrate. A guard electrode and/or ground electrode is formed inside the **ceramic** substrate.

13/3,K/38 (Item 38 from file: 347)

DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

06899613 **Image available**
WAFER PROBER AND **CERAMIC SUBSTRATE** USED FOR THE SAME

PUB. NO.: 2001-127123 [JP 2001127123 A]
PUBLISHED: May 11, 2001 (20010511)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2000-248580 [JP 2000248580]
FILED: August 18, 2000 (20000818)
PRIORITY: 11-233117 [JP 99233117], JP (Japan), August 19, 1999 (19990819)

WAFER PROBER AND **CERAMIC SUBSTRATE** USED FOR THE SAME

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **ceramic** substrate having a chuck top **conduction layer** which can be made thin and has a reduced resistance and excellent adhesion with the **ceramic** substrate.

SOLUTION: This **ceramic** substrate used for a **wafer prober** is obtained by forming a **conductor layer** composed of a plurality of metallic layers.

13/3,K/39 (Item 39 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

06891383 **Image available**
WAFER PROBER AND **CERAMIC** BOARD USED FOR THE SAME

PUB. NO.: 2001-118892 [JP 2001118892 A]
PUBLISHED: April 27, 2001 (20010427)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
FURUKAWA KAZUMASA
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2000-240815 [JP 2000240815]
FILED: August 09, 2000 (20000809)
PRIORITY: 11-227778 [JP 99227778], JP (Japan), August 11, 1999 (19990811)

WAFER PROBER AND **CERAMIC** BOARD USED FOR THE SAME

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
FURUKAWA KAZUMASA

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **wafer prober** which is lightweight, superior in tempera ture rise/fall characteristics, hardly warps when it is ...

... on a silicon wafer, and effectively and accurately measures a wafer without fail.

SOLUTION: A **conductor layer** is formed on the surface of a **ceramic** board which is used for a **wafer prober** , and the **conductor layer** is thinner than the **ceramic** board.

13/3,K/40 (Item 40 from file: 347)

06891382 **Image available**

WAFER PROBER AND **CERAMIC** BOARD USED FOR THE SAME

PUB. NO.: 2001-118891 [JP 2001118891 A]
PUBLISHED: April 27, 2001 (20010427)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
FURUKAWA MASAKAZU
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2000-240814 [JP 2000240814]
FILED: August 09, 2000 (20000809)
PRIORITY: 11-226767 [JP 99226767], JP (Japan), August 10, 1999 (19990810)

WAFER PROBER AND **CERAMIC** BOARD USED FOR THE SAME

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
FURUKAWA MASAKAZU

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **wafer prober** , capable of preventing impurities contained in a chuck top **conductor layer** or a **ceramic** board from being diffused into a silicon wafer.

SOLUTION: A **conductor layer** is formed on a **ceramic** board which is used for a **wafer prober** , and a noble layer is formed on the surface of the **conductor layer** .

13/3,K/41 (Item 41 from file: 347)

06891379 **Image available**

WAFER PROBER AND **CERAMIC** BOARD USED FOR **WAFER PROBER**

PUB. NO.: 2001-118888 [JP 2001118888 A]

PUBLISHED: April 27, 2001 (20010427)
INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
FURUKAWA MASAKAZU
APPLICANT(s): IBIDEN CO LTD
APPL. NO.: 2000-242331 [JP 2000242331]
FILED: August 10, 2000 (20000810)
PRIORITY: 11-226767 [JP 99226767], JP (Japan), August 10, 1999 (19990810)

WAFER PROBER AND **CERAMIC** BOARD USED FOR **WAFER PROBER**

INVENTOR(s): **ITO ATSUSHI**
HIRAMATSU YASUJI
ITO YASUTAKA
FURUKAWA MASAKAZU

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **wafer prober** , which is lightweight, superior in heat-up characteristics and cool-down characteristics, and moreover, does...

... and is suitable to mass production of the prober having a constant quality.

SOLUTION: A **wafer prober** is characterized in that a **conductor layer** is formed on the surface of a polycrystalline **ceramic** board.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 091 400 A1

(12) EUROPEAN PATENT APPLICATION

published in accordance with Art. 158(3) EPC

(43) Date of publication:
11.04.2001 Bulletin 2001/15

(21) Application number: **99949311.7**

(22) Date of filing: **15.10.1999**

(51) Int. Cl.[7]: **H01L 21/66**

(86) International application number:
PCT/JP99/05693

(87) International publication number:
WO 01/06559 (25.01.2001 Gazette 2001/04)

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

(30) Priority: **15.07.1999 JP 20178999**

(71) Applicant: **IBIDEN CO., LTD.**
Ogaki-shi Gifu-ken 503-0917 (JP)

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- **FURUKAWA, Masakazu**
  Ibi-gun, Gifu 501-0695 (JP)

(74) Representative:
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Cabinet Beau de Loménie,
158, rue de l'Université
75340 Paris Cedex 07 (FR)

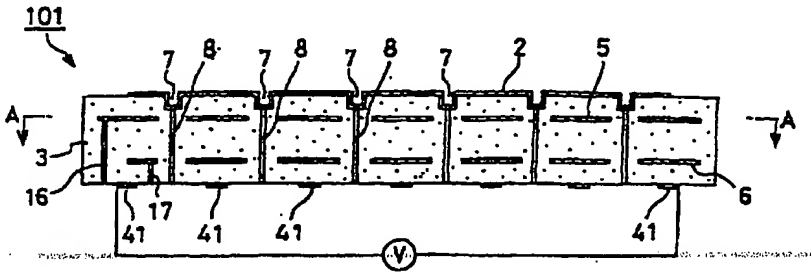
X Priority Document

(54) WAFER PROBER

(57) This invention has its objects to provide a wafer prober which is lightweight, excellent in thermal response kinetics and free from warpage upon pressing with a probe card, thus capable of effective protecting itself against damage to the silicon wafer and measurement error.

This invention is related to a wafer prober wherein a ceramic substrate is formed with a conductor layer on its surface.

Fig. 1



EP 1 091 400 A1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP99/05693

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl' H01L21/66

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl' H01L21/66

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926-1996 Toroku Jitsuyo Shinan Koho 1994-1999
Kokai Jitsuyo Shinan Koho 1971-1999 Jitsuyo Shinan Toroku Koho 1996-1999

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP, 63-151034, A (NEC Corporation), 23 June, 1988 (23.06.88), Claims (Family: none)	8-10
X Y	JP, 62-180944, U (Yukihiko OKADA), 17 November, 1987 (17.11.87), Claims (Family: none)	1-7 8-10

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 December, 1999 (13.12.99)	28 December, 1999 (28.12.99)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)

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=> e 1999jp-201789/ap,apn
'APN' IS NOT A VALID EXPAND FIELD CODE FOR FILE 'PATOSEP'
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'APN' IS NOT A VALID EXPAND FIELD CODE FOR FILE 'PATOSWO'
'APN' IS NOT A VALID EXPAND FIELD CODE FOR FILE 'INPADOC'
E1            2     JP99-201787/AP
E2            2     JP99-201788/AP
E3            2 --> JP99-201789/AP
E4            2     JP99-20179/AP
E5            2     JP99-201790/AP
E6            2     JP99-201791/AP
E7            2     JP99-201792/AP
E8            2     JP99-201793/AP
E9            2     JP99-201794/AP
E10           2     JP99-201795/AP
E11           2     JP99-201796/AP
E12           2     JP99-201797/AP
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=> s e3
L1            2 JP99-201789/AP

=> d bro
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L1    ANSWER 1 OF 2  INPADOC  COPYRIGHT 2004 EPO on STN

PATENT FAMILY INFORMATION
 AN   146999733 INPADOC

 +------------PRAI-------------+      +---------------AI---------------+
 JP 1999-201789       A  19990715      CN 1999-814050       A  19991015
                                       EP 1999-949311       A  19991015
                                       JP 1999-201789       A  19990715
                                       TW 1999-118768       A  19991029
                                       WO 1999-JP5693       A  19991015
 WO 1999-JP5693       W  19991015      EP 1999-949311       A  19991015

 +--------------AI--------------+      +--------------PI--------------+
 CN 1999-814050       A  19991015      CN 1329753           T  20020102
 EP 1999-949311       A  19991015      EP 1091400           A1 20010411
 JP 1999-201789       A  19990715      JP 2001033484        A2 20010209
 TW 1999-118768       A  19991029      TW 449845            B  20010811
 WO 1999-JP5693       A  19991015      WO 2001006559        A1 20010125

 2 priorities, 5 applications, 5 publications
:
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Set     Items   Description
S1      81582   AU=(ITO, A? OR HIRAMATSU Y? OR HIRAMATSU Y? OR ITO A? OR I-
             TO, Y? OR ITO Y? OR FURUKAWA, M? OR FURUKAWA M?)
S2    2755210   WAFER? OR SUBSTRATE? ?
S3    9488027   PROB????
S4    1052325   (CONDUCT??? OR ACTIVE?)(3N)LAYER? OR TRACE?
S5    1096133   CERAMIC?
S6     333405   S2 AND S3
S7        712   S6 AND S4 AND S5
S8         66   S7 AND S1
S9      14916   S2(3N)S3
S10        46   S9 AND S4 AND S5 AND S1
S11        46   RD (unique items)
S12        46   IDPAT (sorted in duplicate/non-duplicate order)
S13        41   IDPAT (primary/non-duplicate records only)
S14     11164   S2(2N)S3
S15       100   S14 AND S4 AND S5
S16        99   RD (unique items)
S17         2   S16 AND PD<=20001221
S18        56   S16 NOT (S17 OR S13)
S19        10   S18 AND PY<=2000
S20        10   RD (unique items)
?  show files
File   2:INSPEC 1969-2004/Oct W1
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         (c) 2004 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2004/Oct W2
         (c) 2004 Inst for Sci Info
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Sep
         (c) 2004 The HW Wilson Co.
File  94:JICST-EPlus 1985-2004/Sep W2
         (c)2004 Japan Science and Tech Corp(JST)
File  92:IHS Intl.Stds.& Specs. 1999/Nov
         (c) 1999 Information Handling Services
File 144:Pascal 1973-2004/Oct W1
         (c) 2004 INIST/CNRS
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         (c) 2004 CMP Media, LLC
File 696:DIALOG Telecom. Newsletters 1995-2004/Oct 15
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File  35:Dissertation Abs Online 1861-2004/Sep
         (c) 2004 ProQuest Info&Learning
File  65:Inside Conferences 1993-2004/Oct W2
         (c) 2004 BLDSC all rts. reserv.
File 103:Energy SciTec 1974-2004/Oct B1
         (c) 2004 Contains copyrighted material
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200465
         (c) 2004 Thomson Derwent
File 347:JAPIO Nov 1976-2004/Jun(Updated 041004)
         (c) 2004 JPO & JAPIO
File 239:Mathsci 1940-2004/Nov
         (c) 2004 American Mathematical Society
File  95:TEME-Technology & Management 1989-2004/Jun W1
         (c) 2004 FIZ TECHNIK
File  25:Weldasearch 1966-2003/Dec
```

20/9/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

01899710 INSPEC Abstract Number: B82043206
Title: The use of hybrid microelectronics in the construction of ion-selective electrodes
Author(s): Leppavuori, S.I.; Romppainen, P.S.
Author Affiliation: Dept. of Electrical Engng., Univ. of Oulu, Oulu, Finland
Conference Title: Proceedings of the Third European Hybrid Microelectronics Conference 1981 p.146-51
Publisher: Internat. Soc. Hybrid Microelectronics Europe, Paris, France
Publication Date: 1981 Country of Publication: France 523 pp.
Conference Date: 20-22 May 1981 Conference Location: Avignon, France
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); Practical (P)
Abstract: The application of hybrid microelectronic manufacturing techniques to the construction of ion-selective electrodes is considered. A solid state pH glass electrode has been manufactured using thick film techniques. The electrode structure studied consists of a **conductive** and a glass **layer** on a **ceramic substrate** . Major **problems** associated with the making of the pH-sensitive glass paste and the choice of **conductive layer** material are discussed. With the correct choice of materials and by using a suitable manufacturing process a linear electrode response can be achieved. (6 Refs)
Subfile: B
Descriptors: chemical variables measurement; electric sensing devices; hybrid integrated circuits; thick film devices
Identifiers: hybrid microelectronics; ion-selective electrodes; solid state pH glass electrode; thick film techniques; **ceramic** substrate; pH-sensitive glass paste; **conductive layer**
Class Codes: B2220J (Hybrid integrated circuits); B7230 (Sensing devices and transducers); B7320T (Chemical variables)

20/9/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011739511 **Image available**
WPI Acc No: 1998-156421/ **199814**
XRPX Acc No: N98-125046
Substrate **structure for** probe **card used in inspection of IC chip under high temperature environment - has** ceramic **layer formed between insulating** layer **and electrically** conductive layer
Patent Assignee: TOHO DENSHI KK (TODE-N)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10027967	A	19980127	JP 96196910	A	19960709	199814	B

Priority Applications (No Type Date): JP 96196910 A 19960709
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10027967	A		4	H05K-003/46	

Abstract (Basic): JP 10027967 A
The structure has an insulating layer (10) and an electrically

conductive layer (7), which are laminated. A **ceramic** layer (15) is formed between the insulating **layer** and the electrically **conductive layer** .

ADVANTAGE - Enables to reduce damage caused due to high temperature. Prevents deformation.

Dwg.2/4

Title Terms: SUBSTRATE; STRUCTURE; PROBE; CARD; INSPECT; IC; CHIP; HIGH; TEMPERATURE; ENVIRONMENT; **CERAMIC** ; LAYER; FORMING; INSULATE; LAYER; ELECTRIC; CONDUCTING; LAYER

Index Terms/Additional Words: LSI

Derwent Class: S01; U11; V04

International Patent Class (Main): H05K-003/46

International Patent Class (Additional): G01R-001/073; H01L-021/66; H05K-001/03

File Segment: EPI

Manual Codes (EPI/S-X): S01-G02B; S01-H03A; U11-F01C1; U11-F01D1; V04-R07A

20/9/3 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

009287521

WPI Acc No: 1992-414932/ **199250**

XRAM Acc No: C92-184119

XRPX Acc No: N92-316474

Conductive compsn. for use on aluminium nitride substrate - comprises copper@ (alloy), glass binder and cadmium@ or an oxide of cadmium

Patent Assignee: FERRO CORP (FECO)

Inventor: BABUDER R F; GARDNER R D; RHOADS K M

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5165986	A	19921124	US 91710559	A	19910605	199250	B

Priority Applications (No Type Date): US 91710559 A 19910605

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5165986	A		7	B32B-009/00	

Abstract (Basic): US 5165986 A

A high thermal conductivity circuit substrate comprises: (a) a sintered aluminium nitride **ceramic** substrate; (b) a conductive pattern bonded to the substrate. It is formed by firing a conductive compsn. comprising: (1) copper or copper alloy; (2) an effective amt. of glass binder; (3) cadmium or an oxide of cadmium; such that the conductive compsn. has been deposited on the substrate, dried and fired to form the pattern bonded to the substrate.

Pref. the Cu alloy comprises Cu and either Al, Ag, Au, Zn, Sn, Pt or mixts. of these. Pref. the glass binder is PbO-2O2-SiO2. Pref. the conductive compsn. comprises a solid and a liq. portion, the solid portion comprising: (i) 80-98% by wt. of Cu or Cu alloy; (ii) 1-10% by wt. of glass binder, (iii) 1-10% by wt. of CdO. Pref. the conductive pattern has an initial adhesion of at least 3.5 lbs. Pref. the conductive pattern is a thin **conductor layer** having a resistivity of 0.1-3.0 ohmns x 10 power (-3). sq.(-1).mil(-1).

USE/ADVANTAGE - Primarily for microcircuit applications and esp. in the power hybrid market where high thermal conductivity is required. Also for resistor and semiconductor pastes, inks, tapes and the like. The substrate combines adequate bond strength with higher thermal

conductivity abnd dielectric strength than e.g. alumina **substrate** ; **problems** of blistering are avoided (claimed).
Dwg. 0/0
Title Terms: CONDUCTING; COMPOSITION; ALUMINIUM; NITRIDE; SUBSTRATE; COMPRISE; COPPER; ALLOY; GLASS; BIND; CADMIUM; OXIDE; CADMIUM
Derwent Class: L03; P73; U11; U14; V04; X12
International Patent Class (Main): B32B-009/00
File Segment: CPI; EPI; EngPI
Manual Codes (CPI/A-N): L03-H04E4; L03-H04E5; L04-C10F; L04-C25
Manual Codes (EPI/S-X): U11-A05B; U11-D01A; U14-H03C; V04-R02P; V04-R05G; X12-D01X

20/9/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009279756 **Image available**
WPI Acc No: 1992-407167/ **199249**
Related WPI Acc No: 1992-381529; 1994-332349
XRAM Acc No: C92-180756
XRPX Acc No: N92-310514
MMIC on ceramic **substrate without stress fracture problems - is grown with** active **and passive buffer** layers **which may be of high temp. superconductor**
Patent Assignee: EATON CORP (EAYT)
Inventor: CALVIELLO J A; HICKMAN G A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5164359	A	19921117	US 90511589	A	19900420	199249	B

Priority Applications (No Type Date): US 90511589 A 19900420
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5164359	A		25	H01L-021/20	

Abstract (Basic): US 5164359 A
A III-V semiconductor MMIC method, with elimination of semi-insulating layer thermal expansion mismatch fracture problems, comprises providing a transparent **ceramic** substrate (12), growing a semi-insulating buffer layer (14) on this which lattice-matches the III-V from these upper layers to the substrate without having to pass otherwise through the semi-insulating layer.
The additional thickness of the semi-insulating layer is eliminated to shorten the thermal conduction path and eliminate the discrete bonding of the semi-insulating layer and substrate. An electro-optic layer is provided on the buffer layer for integration of electro-optic circuitry receiving light through the substrate.
USE/ADVANTAGE - Methods of deposing **active** and passive **layers** on **ceramic** substrates and of forming MMICs (claimed) are provided which are useful for high speed MMICs, and HTS combinations with FETs, MESFETs, HEMTs etc.. Thermal mechanical stress **problems** with **ceramic substrates** are overcome, improving reliability and minimising fractures. Also MMICs may be hermetically sealed by direct bonding and high performance MMICs are obtd..
Dwg.12/23
Title Terms: MMIC; **CERAMIC** ; SUBSTRATE; STRESS; FRACTURE; PROBLEM; GROW; ACTIVE; PASSIVE; BUFFER; LAYER; HIGH; TEMPERATURE; SUPERCONDUCTING
Derwent Class: L03; U14; W02

International Patent Class (Main): H01L-021/20
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L03-A01C; L04-A02; L04-C10F; L04-E01; L04-E01A; L04-E09
Manual Codes (EPI/S-X): U14-F02B; U14-H03C2; U14-H03C3; W02-A01A3

20/9/5 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009091297 **Image available**
WPI Acc No: 1992-218720/ **199227**
XRAM Acc No: C92-098993
XRPX Acc No: N92-166087
Ceramic **substrate for multilayer or printed electronic circuit mfr. - where use of low resistance inexpensive copper@ reduces resistance and expense**
Patent Assignee: MATSUSHITA ELECTRIC IND CO LTD (MATU); MATSUSHITA ELEC IND CO LTD (MATU)
Inventor: ANDO H; KUGIMIYA K; YOKOTANI Y
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 492518	A1	19920701	EP 91121982	A	19911220	199227	B
JP 4221888	A	19920812	JP 90404856	A	19901221	199239	
US 5512353	A	19960430	US 91809985	A	19911218	199623	
			US 94263157	A	19940620		
EP 492518	B1	19970312	EP 91121982	A	19911220	199715	
DE 69125121	E	19970417	DE 625121	A	19911220	199721	
			EP 91121982	A	19911220		

Priority Applications (No Type Date): JP 90404856 A 19901221
Cited Patents: EP 332457; JP 2031906; JP 2225363; JP 2303107; US 4885661; US 5004715; 3.Jnl.Ref; JP 2303107; JP 62031906
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 492518	A1	E	16	H01L-021/48	
Designated States (Regional): DE FR GB					
JP 4221888	A		6	H05K-003/46	
US 5512353	A		12	B32B-009/00	Cont of application US 91809985
EP 492518	B1	E	16	H01L-021/48	
Designated States (Regional): DE FR GB					
DE 69125121	E			H01L-021/48	Based on patent EP 492518

Abstract (Basic): EP 492518 A

A **ceramic** substrate for electronic circuit comprising a **ceramic** and a **conductive layer** , with **ceramic layer** patterned. **Conductive layer** is of Cu or Cu alloy, and **ceramic** layer comprises complex oxide or oxide solid soln. contg. both Cu and a non copper components. **Ceramic** layer is insulated. Method of substrate prodn. comprises: preparing the Cu contg. component and the non copper containing component; forming **ceramic** green sheets; patterning a **conductive layer** comprising binder and Cu oxide; laminating the **ceramic** green sheets to form a laminated body; heating the laminated body in air to burn out the binder; heating the laminated body in reducing gas to reduce and metallize the **conductive layer** ; firing the laminated body in inert gas to sinter the **ceramic** .

USE/ADVANTAGE - A **ceramic** substrate for electronic circuit using a special composition **ceramic** layer for multilayer electronic circuit or for an insulated layer in a **ceramic** substrate for printed

electronic circuit. Use of inexpensive Cu of low resistance used as a **conductive layer** in a **ceramic substrate** overcomes **problems** of high electric resistance and expense associated with other elements.

Dwg.1A/5

Abstract (Equivalent): EP 492518 B

A **ceramic** substrate for electronic circuit comprising a sintered **ceramic** substrate, a **conductive layer** which is patterned on the **ceramic** substrate and comprises copper or an alloy containing copper as its main component, at least one insulating layer formed so as to cover a portion of the **conductive layer** , and another **conductive layer** which is patterned at least on the insulating layer and comprises copper or an alloy containing copper as its main component, wherein the insulating layer consists of a complex oxide or an oxide solid solution containing oxygen, copper and at least one element other than copper, but contains no metallic copper on separate copper oxide phases, whereby the diffusion rate of copper oxide from the **conductive layers** to the insulating layers can be lowered.

Dwg.1B/2C

Abstract (Equivalent): US 5512353 A

A **ceramic** substrate for a multilayered electronic circuit comprises a number of **ceramic** insulated layers, and a number of **conductive layers** which are patterned on the **ceramic** layers, the **ceramic** insulated **layers** and **conductive layers** being laminated alternately, where the **conductive layers** comprise metallic copper or an alloy contg. metallic copper as its main component, and where the **ceramic** layers entirely comprise a complex oxide or an oxide solid soln. contg. copper and at least one component other than copper, where the complex oxide or the oxide solid soln. is prepd. by using oxide contg. copper as a starting material, whereby the diffusion rate of the copper oxide from the **conductive layers** to the **ceramic** layers can be lowered, and where each of the complex oxide and the oxide solid soln. contains at least one element selected from the gp. A consisting of strontium, barium, calcium, and lead, and at least one element selected from the gp. B consisting of tungsten, niobium, and tantalum, so as to form a complex perovskite structure phase.

Dwg.0/2

Title Terms: **CERAMIC** ; SUBSTRATE; MULTILAYER; PRINT; ELECTRONIC; CIRCUIT; MANUFACTURE; LOW; RESISTANCE; INEXPENSIVE; COPPER; REDUCE; RESISTANCE; EXPENSE

Derwent Class: L03; U11; U14; V04

International Patent Class (Main): B32B-009/00; H01L-021/48; H05K-003/46

International Patent Class (Additional): C04B-037/02; H01L-023/15; H05K-001/09; H05K-003/38

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L03-H04E3; L03-H04E5; L03-J; L04-C22

Manual Codes (EPI/S-X): U11-D01A; U14-H03B1; U14-H04A3; V04-R07A; V04-R07L

20/9/6 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

007218063

WPI Acc No: 1987-215071/ **198731**

XRPX Acc No: N87-160812

Wafer probe for individual chip testing - has end shaped to permit close approach to component under test and has amplifier mounted on that end

Patent Assignee: TEKTRONIX INC (TEKT); TRIQUINT SEMICONDUC (TRIQ-N)

Inventor: FLEASON R; FLEGAL R T; MCCAMANT A J; STRID E W

Number of Countries: 007 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 230766	A	19870805	EP 86309951	A	19861219	198731	B
JP 62190738	A	19870820	JP 86307570	A	19861223	198739	
CA 1252221	A	19890404				198918	
US 4853627	A	19890801	US 88217107	A	19880711	198938	

Priority Applications (No Type Date): US 85812480 A 19851223
Cited Patents: EP 131375; US 4161692
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 230766	A	E	7		
Designated States (Regional): DE FR GB NL					
US 4853627	A		5		

Abstract (Basic): EP 230766 A

The triangular **ceramic** wafer (4) has a high input impedance monolithic integrated circuit amplifier (8) formed at the apex. The amplifier input (28) is connected to a conductive probe (30) for contacting a node of a circuit under test.

The amplifier output is connected to a measurement and display instrument by a transmission line formed by a microstrip (24) and a **conductive layer** (22) on the underside of the wafer.

ADVANTAGE - Due to high amplifier input impedance, operation of circuit under test is not disturbed

Abstract (Equivalent): US 4853627 A

A **wafer probe** comprises a support member having an end region which is shaped to permit the end region to be brought into close proximity with a component under test. An amplifier is mounted on the support member at its end region. A conductive probe element is attached to the amplifier and is electrically connected to the amplifier's input terminal.

A transmission line is connected to the amplifier's output terminal for transmitting signals form the amplifier to a measurement instrument.

USE/ADVANTAGE - Testing individual chips prior to dicing and packaging without significantly disturbing signal level at probed pads

Title Terms: WAFER; PROBE; INDIVIDUAL; CHIP; TEST; END; SHAPE; PERMIT; CLOSE; APPROACH; COMPONENT; TEST; AMPLIFY; MOUNT; END
Derwent Class: S01; U11
International Patent Class (Additional): G01R-001/06; G01R-031/28; H01L-021/66
File Segment: EPI
Manual Codes (EPI/S-X): S01-G02; S01-G04; S01-H03; U11-F01D1

20/9/7 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007054119 **Image available**
WPI Acc No: 1987-054116/ **198708**
XRAM Acc No: C88-091768
XRPX Acc No: N88-156961
Electroluminescent device with monolithic ceramic **substrate - high dielectric constant** ceramic **gives strength and freedom from breakdown**
Patent Assignee: NEC CORP (NIDE)
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week

JP 62010898 A 19870119 198708 B
US 4757235 A 19880712 US 86857374 A 19010101 198830

Priority Applications (No Type Date): JP 85148617 A 19850705; JP 8592884 A 19850430
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
JP 62010898 A 13

Abstract (Basic): JP 62010898 A

An electroluminescent device comprises a monolithic substrate (10) with embedded internal electrodes (12) and a multilayer thin film structure (40) which includes a luminescent layer (14) sandwiched between transparent electrode layers (16) and the substrate (10). The substrate (10) is formed by sintering laminated **ceramic** green sheets of a dielectric constant greater than 200 with a **conductive** paste **layer** between them. Insulating layers (13, 15) are sandwiched between the internal electrodes (12) and luminescent layer (14) and between this layer (14) and the transparent electrode (16). In another embodiment a second thin insulator layer is provided between luminescent layer (14) and substrate (10) to prevent ionic diffusion into the former (14).

The substrate is provided with an external terminal at the bottom connected to the internal electrodes (12). The luminescent layer (14) consists of ZnS:Mn or ZnS:TbF3 or ZnS:SmF3 and the insulating layer (13) of a stable oxide of Si3N4 or CaF2.

USES/ADVANTAGES - Existing glass-based electroluminescent devices may suffer from dielectric breakdown **problems** . **Ceramic substrates** have been proposed but previously have been mechanically weak. The present invention uses a reliable sintered multilayer **ceramic** plate with internal electrode as substrate which gives rise to devices of high brightness at low driving current and high reliability and stability against dielectric breakdown. (First major country equivalent to J62010898-A)

2/9

Abstract (Equivalent): US 4757235 A

An electroluminescent device comprises a monolithic substrate (10) with embedded internal electrodes (12) and a multilayer thin film structure (40) which includes a luminescent layer (14) sandwiched between transparent electrode layers (16) and the substrate (10). The substrate (10) is formed by sintering laminated **ceramic** green sheets of a dielectric constant greater than 200 with a **conductive** paste **layer** between them. Insulating layers (13, 15) are sandwiched between the internal electrodes (12) and luminescent layer (14) and between this layer (14) and the transparent electrode (16). In another embodiment a second thin insulator layer is provided between luminescent layer (14) and substrate (10) to prevent ionic diffusion into the former (14).

The substrate is provided with an external terminal at the bottom connected to the internal electrodes (12). The luminescent layer (14) consists of ZnS:Mn or ZnS:TbF3 or ZnS:SmF3 and the insulating layer (13) of a stable oxide of Si3N4 or CaF2.

USES/ADVANTAGES - Existing glass-based electroluminescent devices may suffer from dielectric breakdown **problems** . **Ceramic substrates** have been proposed but previously have been mechanically weak. The present invention uses a reliable sintered multilayer **ceramic** plate with internal electrode as substrate which gives rise to devices of high brightness at low driving current and high reliability and stability against dielectric breakdown. (First major country equivalent to J62010898-A) (13pp Dwg.No.2/9)

Title Terms: ELECTROLUMINESCENT; DEVICE; MONOLITHIC; **CERAMIC** ; SUBSTRATE; HIGH; DIELECTRIC; CONSTANT; **CERAMIC** ; STRENGTH; FREE; BREAKDOWN
Derwent Class: L03; U14
International Patent Class (Additional): H05B-033/22
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L03-G05; L03-H04; L03-H04A
Manual Codes (EPI/S-X): U14-H03B; U14-J

20/9/8 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003465585
WPI Acc No: 1982-13529E/ **198207**
Large area multilayer printed circuit - has alternate thick film dielectric and conductor layers **on molybdenum substrate**
Patent Assignee: GENERAL ELECTRIC CO (GENE)
Inventor: BARNES N S; MOGLE R A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4313262	A	19820202				198207	B

Priority Applications (No Type Date): US 79103984 A 19791217
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4313262	A		4		

Abstract (Basic): US 4313262 A
Large area multilayer printed circuit structure is made by (a) providing an Mo substrate (2); (b) screen printing a dielectric layer (20) and allowing to dry; (c) firing; (d) repeating (b,c) until the required thickness of dielectric is formed; (e) screen printing a first conductor circuit (24) on the dielectric surface and allowing to dry; (f) firing; (g) screen printing a second dielectric layer (26,27) on the conductor and first dielectric and allowing to dry; (h) firing; and (i) repeating (e,f,g,h) until the required number of dielectric-**conductor layers** are formed.
Pref., components (32,34) are bonded or soldered to the top surface of the structure, and thus interconnected to at least one exposed conductor.
The structure is thinner than conventional yet has the required rigidity. It can be automatically processed without size constraints or camber **problems** . The Mo **substrate** acts as a heat sink and/or bottom cover of a hermetic package, avoiding metallisation and soldering needed for **ceramic** substrates; has an expansion coefft. matched to the dielectric and **ceramic** chip carriers; and can be fired at hiqh temps. compatible with low cost Cu conductors.
2
Title Terms: AREA; MULTILAYER; PRINT; CIRCUIT; ALTERNATE; THICK; FILM; DIELECTRIC; CONDUCTOR; LAYER; MOLYBDENUM; SUBSTRATE
Derwent Class: L03; U14; V04
International Patent Class (Additional): H05K-003/34
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L03-H04E
Manual Codes (EPI/S-X): U14-H02; V04-R05

20/9/9 (Item 1 from file: 347)

DIALOG(R)File 347:JAPIO

04596135 **Image available**
MICRO PROBER

PUB. NO.: 06-268035 [JP 6268035 A]
PUBLISHED: September 22, 1994 (**19940922**)
INVENTOR(s): NAKANO KATSUYOSHI
APPLICANT(s): EEJINGU TESUTA KAIHATSU KYODO KUMIAI [000000] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 05-087721 [JP 9387721]
FILED: March 10, 1993 (19930310)
INTL CLASS: [5] H01L-021/66; G01R-001/073
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components); 46.1 (INSTRUMENTATION -- Measurement); 46.2 (INSTRUMENTATION -- Testing)
JOURNAL: Section: E, Section No. 1647, Vol. 18, No. 673, Pg. 46, December 19, 1994 (19941219)

ABSTRACT

PURPOSE: To enable simultaneous probing to pad portions of a plurality of specimens formed on a semiconductor substrate.

CONSTITUTION: Electric circuits consisting of a conductive material film or **conductive layer** is formed on a **prober substrate** 1 consisting of semiconductor such as silicon and materials which assure good reproducibility to stress and have small thermal expansion coefficient such as ceramic or metal with coating of insulating film. A comb-teeth portion having the layout and size accurately corresponding to a pad portion 8' of an IC (semiconductor integrated circuit) element which is formed on the surface of a silicon substrate as an inspection sample obtained by processing the **prober substrate** 1 is also provided and a projected metal part is also formed on the electric circuit at the end part of the comb-teeth portion as a contact for the pad portion 8' of the specimen Moreover, the probing with a plurality of inspection samples can be made simultaneously by providing a plurality pairs of probing portions through modification of thickness, size, shape, composition and property in the pitch matching with the arrangement of the specimen in order to give necessary mobility to the comb-teeth portion and the periphery thereof.

20/9/10 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

02985229 **Image available**
WAFER PROBER

PUB. NO.: 01-282829 [JP 1282829 A]
PUBLISHED: November 14, 1989 (**19891114**)
INVENTOR(s): SATO TERUYA
YAMAGUCHI ATSUHITO
UKAJI TAKAO
OMORI TARO
MURAKAMI EIICHI
APPLICANT(s): CANON INC [000100] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-111458 [JP 88111458]
FILED: May 10, 1988 (19880510)
INTL CLASS: [4] H01L-021/66
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)

JOURNAL: Section: E, Section No. 883, Vol. 14, No. 62, Pg. 66, February 05, 1990 (19900205)

ABSTRACT

PURPOSE: To ensure all electric contact, and to improve the accuracy of positioning by image-sensing the tip of a probing needle, deciding the state of the tip and conducting the suspension of a test and the correction operation of a defective needle point when a defective state such as fouling, cracking, etc., is detected.

CONSTITUTION: A contact plate 21 is lifted by a pulse motor 62 through an arm holder 60 to a position in the Z direction of a needle point. The needle point section of a probing needle 6 is lit through the plate 21 by a high brightness LED 23 under the state, and the needle point is image-sensed by a TV camera 20. When it is confirmed that keeping within a needle **trace** tolerance of all needle points is impossible even by revolution, the adhesion of aluminum chips to the needle point is decided. A **ceramic** board 28 is positioned under the needle point by moving an XY stage 3, and the Z stage section of a .theta.Z stage 2 is shifted vertically so that the needle point is overdriven, thus polishing the needle point. Accordingly, an electric contact is ensured, and the accuracy of positioning is improved.
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